REMARKS

Present Status of the Application

Applicants appreciate that the Office Action consider claims 5 and 8 to be allowable.

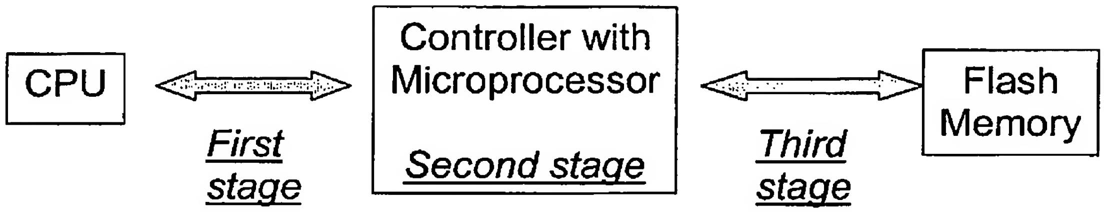
The Office Action rejected claims 1, 3, 4, 6, 7 and 23 under 35 U. S. C. 102(e) as being anticipated by Roohparvar (U. S. Patent 6,851,026). The Office Action also rejected claims 9-15 under 35 U. S. C. 102(b) as being anticipated by Fandrich et al. (U. S. Patent 5,519,847; Fandrich). Applicants have amended independent claim 1 to further recite the allowable features in allowable claim 5. Allowable dependent claim 8 has been amended as an independent claim. The claim dependency has been accordingly amended, too. Claims 1, 4, 6-10 and 12-15 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Rejections from Office Action

1. The Office Action rejected claims 1, 3, 4, 6, 7 and 23 under 35 U. S. C. 102(b) as being anticipated by Roohparvar. Applicants have amended independent claim 1 to recite the features in allowable claim 5. Applicants have also rewritten allowable claim 8 as an independent claim. Claims 1, 4 and 6-8 are now in condition for allowance.

2. The Office Action also rejected claims 9-15 under 35 U. S. C. 102(b) as being anticipated by Fandrich. Applicants respectfully traverse the rejections for at least the reasons set forth below.

It should be noted that the three stages in the present invention has the following relation:

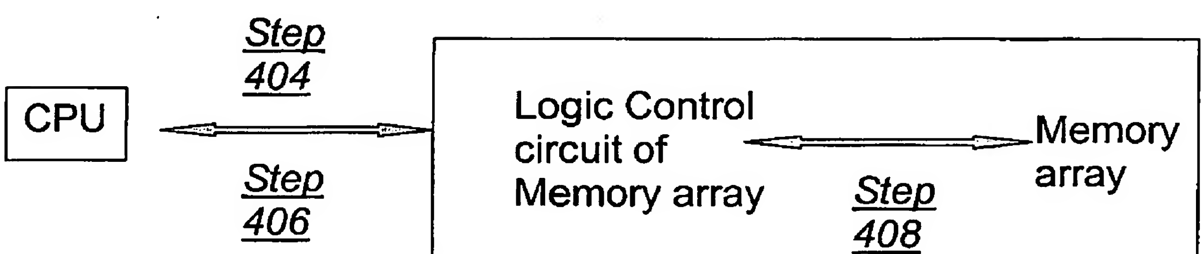


The functions of the CPU, controller and flash memory of the system above are described in page 1, lines 16-21 and the descriptions of the three stages are in page 21, lines 4-10. In the first stage, the microprocessor issues a request to the CPU for data transfer, causing the CPU to transfer a sector of data to the buffer. It relates to the control and access operations between controller and CPU. In the second stage, the microprocessor in the controller computes for the address of the sector where the data are to be written into. It relates to the operation inside the controller. In the third stage, a write request is issued to write data into the flash memory. It relates to the access operation between controller and flash memory.

The Office Action in "***Response to Argument***" refers "Give Program Command" to the second stage of the present invention. Applicants respectfully disagree.

In Fig.6, step 404 and step 406 show that both steps relate to the control and access operation between CPU and the logic control circuit of memory array. The operation in step 404 is "Give Flash Memory a "Page Buffer Write Sequential Command" for Available Plane". In step 406, the access operation is "Load/Write Data into Page Buffer via User Data Bus". Apparently, the operations of "Load Plane A & Give Program /Command" in time line 430 relates to the

control and access operations between CPU and the logic control circuit of memory array. It should be considered as the first stage of the present invention. Apparently, ***the step 404 is not the second stage of the present invention***. Moreover, Frandrich didn't teach the overlapping features of the second stage with other stages. The diagram below can show the corresponding partitions. The step 408 of Fig.6 is "Command Flash Memory Device to Program Memory Array From Page Buffer" which is corresponding to time line 450 of "Program from Plane A" of Fig.8. This step relates to the access operation between memory array and the logic control circuit of the memory array. It should be considered as the third stage of the current invention. The three steps 404, 406, and 408 can be summarized in the following drawing.



Therefore, Fandrich failed to disclose the features recited in independent claim 9.

Applicants respectfully submit that independent claims 1, 8, and 9 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 4, 6-7, 10, and 12-15 patently define over the prior art references as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1, 4, 6-10 and 12-15 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 1/27/2006

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